09/836,286

Abstract of the disclosure

A method of manufacturing a semiconductor device having a multi-layer wiring structure including a photo-resist pattern having a prescribed opening dimension which is formed on an interlayer insulating film composed of an organic low dielectric constant film and a silicon-containing insulating film durable to an NH_3-based gas wherein the silicon-containing insulating film is dry etched using the photo-resist pattern as a mask and then the organic low dielectric constant film is etched by dry etching with NH_3 or an NH_3-containing gas using the silicon-containing insulating film as an etching mask to form an opening part having a high aspect ratio and a substantially vertical cross-section shape. The described method prevents bowing of the cross-section shape of a via hole formed in an organic low dielectric constant film as well preventing a shoulder drop effect in a silicon-containing insulating film used as an etching mask for the organic low dielectric constant film and provides a method for fabricating the semiconductor device which is capable of etching the organic low dielectric constant film with a high amount of precision.